IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 7, 10 and 13, and AMEND claims 1, 2, 4-6, 8, 9, 11, 12, 14 and 15 and ADD claim 16 in accordance with the following:

1. (Currently Amended) A timing analysis apparatus for performing timing analysis of a semiconductor integrated circuit based on inputted circuit information, comprising:

a first timing analysis unit performing timing analysis in a target path which is an analysis target in the semiconductor integrated circuit by accumulating a variation in delay time of each gate in the target path, based on circuit information;

a determination unit determining whether previously specified timing conditions are satisfied or not based on a result of the timing analysis supplied from said first timing analysis unit;

a coefficient arithmetically operating unit ~~for~~ calculating variation coefficients of delay time in ~~a~~ the target path ~~being an analysis target~~ with ~~a~~ the variation in the delay time ~~in~~ of each gate being cancelled out in accordance with a number of gate stages in the target path only when it is determined that the timing conditions are not satisfied in said determination unit ~~in the semiconductor integrated circuit~~; and

a ~~first~~ second timing analysis unit ~~for~~ performing timing analysis in the target path based on the circuit information and the ~~calculated~~ variation coefficients ~~and the circuit information~~calculated by said coefficient arithmetically operating unit.

2. (Currently Amended) The timing analysis apparatus according to claim 1, wherein said coefficient arithmetically operating unit further comprises:

a coefficient of the number of stages arithmetically operating section ~~for~~ calculating coefficients of the number of stages indicating variation amounts in delay time according to the number of gate stages in the target path based on the circuit information;~~,~~

a variation width arithmetically operating section ~~for~~ calculating a variation width of delay time in the entire target path based on the circuit information~~,~~; and

a variation coefficient arithmetically operating section ~~for~~ calculating the variation coefficients of the delay time in the target path based on the calculated coefficients of the number of stages and the variation width of the delay time.

3. (Original) The timing analysis apparatus according to claim 2, further comprising:

a table of coefficients of the number of stages in which an optional number of gate stages in a path and the coefficients of the number of stages are made to correspond to each other,

wherein said coefficient of the number of stages arithmetically operating unit obtains the coefficients of the number of stages according to the number of gate stages in the target path with reference to said table of the coefficients of the number of stages.

4. (Currently Amended) The timing analysis apparatus according to claim 1, further comprising:

an information input unit ~~for~~ inputting the circuit information therein and extracting delay information relating to delay time of each gate in the target path from the circuit information,

wherein said coefficient arithmetically operating unit calculates the variation coefficients of the delay time in the target path based on the extracted delay information of each gate.

5. (Currently Amended) The timing analysis apparatus according to claim 1, wherein:

said first timing analysis unit verifies whether previously specified timing conditions are satisfied in the target path or not, based on the calculated variation coefficients and the circuit information.

6. (Currently Amended) The timing analysis apparatus according to claim 5, wherein:

the timing conditions are the conditions relating to setup time and hold time in the target path.

7. (Canceled)

8. (Currently Amended) The timing analysis apparatus according to claim ~~7~~1, further comprising:

an information input unit ~~for~~ inputting the circuit information therein and extracting delay information relating to the delay time of each gate in the target path,

wherein said second timing analysis unit performs timing analysis of the target path based on the extracted delay information of each gate.

9. (Currently Amended) A timing analysis method for performing timing analysis of a semiconductor integrated circuit based on inputted circuit information, comprising:

a delay information extracting step of ~~having the circuit information inputted and~~ extracting, from the inputted circuit information, delay information relating to delay time of each gate in a target path ~~being~~ constituting an analysis target in the semiconductor integrated circuit from the circuit information;

a first timing analysis step of performing timing analysis in the target path by accumulating the variation in the delay time of each gate in the target path based on the delay information extracted in said delay information extracting step;

a determination step of determining whether previously specified timing conditions are satisfied or not, based on an analysis result in said first timing analysis step;

a coefficient arithmetically operating step of calculating variation coefficients of the delay time of each gate in the target path with a variation in the delay time ~~in~~ of each gate being cancelled out in accordance with the number of gate stages in the target path, based on the delay information extracted in said delay information extracting step, said coefficient arithmetically operating step is executed only when it is determined that the timing conditions are not satisfied in said determination step; and

a ~~first~~ second timing analysis step of performing timing analysis in the target path ~~with use of the~~based on the circuit information and the calculated variation coefficients calculated in said coefficient arithmetically operating step ~~and the circuit information~~.

10. (Cancelled)

11. (Currently Amended) The timing analysis method according to claim 9, wherein:

said coefficient arithmetically operating step comprises a coefficient of a number of stages of arithmetically operating steps of calculating coefficients of a number of stages showing variation amounts of delay times according to the number of gates in the target path, based on the circuit information;

a variation width arithmetically operating step of calculating a variation width of delay time of the entire target path, based on the circuit information; and

a variation coefficient arithmetically operating step of calculating the variation coefficients of the delay time in the target path, based on the coefficients of the number of stages calculated in said coefficient of the number of stages arithmetically operating step and the variation width of the delay time calculated in said variation width arithmetically operating step.

12. (Currently Amended) A computer-readable recording medium recording a program ~~product for making a~~for controlling a computer to execute:

a delay information extracting step of extracting delay information relating to delay time of each gate in a target path ~~being~~ constituting an analysis target in a semiconductor integrated circuit from circuit information of the semiconductor integrated circuit;

a first timing analysis step of performing timing analysis in the target path by accumulating a variation in the delay time of each gate in the target path, based on the delay information extracted in said delay information extracting step;

a determination step of determining whether previously specified timing conditions are satisfied or not, based on an analysis result in said first timing analysis step;

a coefficient arithmetically operating step of calculating variation coefficients of delay time in the target path with ~~a~~ the variation in the delay time ~~in~~ of the each gate being cancelled out in accordance with a number of gate stages in the target path, based on the delay information extracted in said delay information extracting step, only when it is determined that the timing conditions are not satisfied in said determination step, said program product makes the computer execute said coefficient arithmetically operating step; and

a ~~first~~ second timing analysis step of performing timing analysis in the target path based on the circuit information and the calculated ~~with use of the~~ variation coefficients calculated in said coefficient arithmetically operating step ~~and the circuit information~~.

13. (Cancelled)

14. (Currently Amended) The computer-readable recording mediumprogram product according to claim 12, wherein:

said coefficient arithmetically operating step comprises a coefficient of a number of stages of arithmetically operating steps of calculating coefficients of a number of stages indicating variation amounts of delay time according to the number of gate stages in the target path, based on the circuit information;

a variation width arithmetically operating step of calculating a variation width of delay times in the entire target path, based on the circuit information; and

a variation coefficient arithmetically operating step of calculating the variation coefficients of the delay time in the target path, based on the coefficients of the number of stages calculated in said coefficient of the number of stages arithmetically operating step and the variation width of the delay time calculated in said variation width arithmetically operating step.

15. (Currently Amended) The computer-readable recording mediumprogram product according to claim 14, wherein:

the coefficients of the number of stages according to the number of gate stages in the target path is obtained with reference to a table of the coefficient of the number of stages with an optional number of gate stages in a path and the coefficient of the number of stages being made to correspond to each other, recorded in a the recording medium.

16. (New) A timing analysis apparatus performing timing analysis of a semiconductor integrated circuit based on inputted circuit information, comprising:

a controller:

performing timing analysis in a target path in the semiconductor integrated circuit by accumulating a variation in delay time of each gate in the target path,

determining whether previously specified timing conditions are satisfied based on a result of the performed timing analysis,

performing timing analysis in the target path based on calculated variation coefficients of delay time in the target path with the variation in the delay time of each gate being cancelled out in accordance with a number of gate stages in the target path, only when said timing conditions are not satisfied.